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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,171	10/08/2003	Tom Teng	M4065.0925/P925	5786

24998 7590 09/20/2006

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
MARTINEZ, DAVID E	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,171	TENG, TOM	
	Examiner	Art Unit	
	David E. Martinez	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *1-12,18 and 23-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/15/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species 9 – Figure 8 (with the selection of claims 1-8, 11-17, 19-22, 28-29, 32-33 and 55-62 as reading on the selected species) in the reply filed on 6/27/06 is acknowledged. However, the Examiner respectfully disagrees with the selection of those claims as reading on Species 9 (fig. 8). Independent Claims 1, 13, 28 and 55 are directed to different embodiments of different scope. Claim 1 differs from claims 13, 28 (claim 28 and 29), 55 and figure 8, by only reciting one buffer that is only required to output to a second device one of the request signal or the reply signal that were previously received by buffer from the first device. Claim 1 showing only 1 buffer, does not necessarily read on figure 8 nor does it recite all the elements that independent claims 13 and 28 have. The part reciting at least one buffer reads more on figure 7b in combination with figure 8. The same that was said for claim 1 can be said for claim 55. In addition to the group of claims 55-62, it differs from the other claims in that it requires the performing of a search operation (claim 60) and it must insert a search hit index into said second reply signal (claim 61) which is not required by the other selected claims.

As per claim 28, it differs from the other claims by not requiring the first device receiving a request signal from a first source nor that same first device having a second input for receiving a first reply signal from said first source.

Upon review/comparison of Applicant's elected claims and figure 8, and for the above reasons, claims 13-17 and 19-22 are being presented as examined and claims 1-8, 11-12, 28-29, 32-33 and 55-62 are being withdrawn from consideration along with the other non-elected claims due to the election without traverse of species 9 directed to figure 8.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14,16,17, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 14, the term "an output bus coupled between said first and second buffers and a second device" renders the claim indefinite. It isn't clear if the term refers to one output bus coming out of each of the first and second buffers (i.e. two separate output busses connecting each buffer to the second device), or if it is only one output bus connecting both buffers to the second device.

With regards to claims 16,17 and 21, due to their dependency from claim 14, they suffer from the same deficiencies and thus are rejected under the same rationale.

With regards to claim 20, the use of the word "may" in line 2 renders the claim indefinite since it isn't clear if the operation the word is referring to is being performed or not, or if it's an optional feature to the system. The system either bypasses buffer stages or it doesn't, you can't do both.

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-17 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of US Patent Application Publication No. US 2004/0022082 A1 to Khanna.

1. With regards to claim 13, AAPA teaches a system of cascaded devices, comprising:

a first device [element D_i] having a first input for receiving a request signal from a first source [every element in the cascaded series of elements D_{0+1} to D_{n-1} has an input port for receiving a request signal from its previously cascaded element over bus b_i], a second input for receiving a first reply signal from said first source [every element in the cascaded series of elements D_{0+1} to D_{n-1} has an input port for receiving a reply signal from its previously cascaded element over bus B_i], a first output for outputting said request signal [request output port in element D_i for sending a request over bus element b_i to cascaded element D_{i+1}], and a second output for outputting a second reply signal [reply output port in element D_i for sending a reply over bus element B_i to cascaded element D_{i+1}];

AAPA teaches all of the above limitations but is silent as to a first programmable buffer coupled to said first device for receiving said outputted request signal; and a second programmable buffer coupled to said first device for receiving said second reply signal. However, Khanna teaches a first programmable buffer [figs 2,3 element 225] coupled to a first device [fig 2 element 221] for receiving an outputted signal [fig 2 signals sent over lines 210], and a second programmable buffer [figs 2,3 element 225] coupled to a first device [fig 2 element 221] for receiving a second signal [cascade register element 225 includes a plurality of storage elements – see paragraphs 26-28] before relaying the signals to an adjacent (cascaded) second device (fig 2 element 223) for the benefit of reducing both the signal flight distance and the

charge transfer required to stabilize a signal along the length of a given signal line [paragraph 30].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of AAPA and Khanna to have a first programmable buffer coupled to said first device for receiving said outputted request signal; and a second programmable buffer coupled to said first device for receiving said second reply signal for the benefit of reducing both the signal flight distance and the charge transfer required to stabilize a signal along the length of a given signal line.

2. With regards to claim 14, the combination of AAPA and Khanna teaches the system of claim 13, further comprising an output bus [fig 2 output signal elements 211 – paragraph 26-28] coupled between said first [Khanna fig 2, element 225] and second buffers [Khanna fig 2, element 225] and a second device [fig 2 element 223] for the same benefits as those set forth above in claim 13 thus rejected under the same rationale.

3. With regards to claim 15, AAPA teaches the system of claim 13, wherein said second reply signal is generated from said request signal and said first reply signal [paragraph 6].

4. With regards to claim 16, AAPA teaches the system of claim 14, wherein said first buffer buffers said outputted request signal when said second device has a lower latency than said first device [paragraph 5].

5. With regards to claim 17, AAPA teaches the system of claim 14, wherein said second buffer buffers said second reply signal when said second device has a higher latency than said first device [paragraph 5].

6. With regards to claim 21, the combination of AAPA and Khanna teaches the system of claim 14, wherein said first device [AAPA paragraph 5 or Khanna fig 2 element 221] and said

second device [AAPA paragraph 5 or Khanna fig 2 element 223] are content addressable memory (CAM) devices [Khanna paragraph 26].

7. With regards to claim 22, the combination of AAPA and Khanna teaches the system of claim 13, wherein said first and second programmable buffers are part of a same buffer unit [Khanna fig 2 element 225, paragraphs 27, 28].

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of US Patent Application Publication No. US 2004/0022082 A1 to Khanna and further in view of US Patent No. 5,978,355 to Yamaguchi.

8. With regards to claim 19, the combination of AAPA and Khanna are silent as to the system of claim 13, wherein said first buffer and said second buffer have programmable depths. However, Yamaguchi teaches using buffers with programmable depths for the benefit of preventing buffer overflow and underflow [abstract].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of AAPA, Khanna and Yamaguchi to have said first buffer and said second buffer have programmable depths for the benefit of preventing buffer overflow and underflow.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of US Patent Application Publication No. US 2004/0022082 A1 to Khanna in view of US Patent No. 5,978,355 to Yamaguchi and further in view of US Patent No. 5,956,492 to Jander et al. (hereinafter Jander)

9. With regards to claim 20, the combination of AAPA, Khanna and Yamaguchi is silent as to the system of claim 19, wherein buffer stages in said first buffer and said second buffer may be bypassed. However, Jander teaches the use of buffers that have buffer stages that are be bypassed for the benefit of having data reach the front of the buffer faster and thus data latency

or time needed for data to fall-through the buffer are minimized [column 1 lines 10-32 and lines 54-57].

It would have been obvious to one of ordinary skill in the art to combine the teachings of AAPA, Khanna, Yamaguchi and Jander to have the buffer stages in said first buffer and said second buffer may be bypassed for the benefit of having data reach the front of the buffer faster and thus data latency or time needed for data to fall-through the buffer are minimized.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. US 20040024960A1 to King et al. teaches multiple CAM networks and cascaded CAM devices, each having dual inputs and dual outputs.

US Patent No. 5,930,359 to Kempke et al. teaches cascaded CAM devices having buffers interconnecting them.

US Patent No. 7,058,757 to Branth et al. teaches cascaded cam devices having buffers interconnecting them.

US Patent No. 5,640,515 to Park teaches using a buffer for rate matching between two devices.

US Patent No. 6,606,666 to Bell, Jr. et al. teaches buffering data between a sender and a receiver for controlling data flow

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DEM

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/15/2006